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App Note 365: DS3134 CHATEAU Initialization Steps

Application Note 365 provides the initialization steps of the Dallas Semiconductor/Maxim DS3134 CHATEAU HDLC controller.

Overview

By design, upon power on Chateau will not take control of the PCI bus. All the physical ports (port 0 to 15) will send all ones (not HDLC idle code) therefore CHATEAU will be idle upon power on. On the other hand Chateau utilizes RAM base memory, direct and indirect, to store the states of the internal state machines states. Because there are many very complex state machines and inter-working functional blocks of CHATEAU, therefore upon power on all these internal Registers/RAMs must be initialized to a known state before any data packets can be transmitted and received.

It is recommended that users follow this initialization sequence before sending packet data.

Initialization Steps

Initialization Step	Comments
1. System reset.	System reset can be invoked by either hardware action via the PRST* signal or software action via the RST control bit in the Master Reset and ID register. All configuration registers are set to zero (0000h) by system reset.
2. Configure Local Bus Bridge Mode Control register (LBBMC),if CHATEAU is use in bridge mode.	Please note that this register is not affected by software invoked system reset. It will be forced to all zeros only by the hardware reset.
3. Initialize the PCI Configuration Registers.	Achieved by asserting the PIDSEL signal.
4. Initialize All Indirect Registers.	All indirect registers need to be initialized to 0000h. See Table 1 below for a list of all indirect registers.

5. Configure the Device for Operation.	Program all of the necessary registers, which includes the Layer One, HDLC, FIFO, and DMA registers. Except: Leave the TFDA1 bits set to 0 (default state) for all transmit ports (TP[n]CR).
6. Enable the HDLC Channels.	Accomplished via the RCHEN and TCHEN bits in the R[n]CFG[j] and T[n]CFG[j] registers.
7. Load the DMA Descriptors.	Indicate to the DMA where packet data can be written and where pending data (if any) resides
8. Enable the DMAs.	Accomplished via the RDE and TDE control bits in the Master Configuration (MC) register.
9. Enable DMA for each HDLC Channel.	Accomplished via the Channel Enable bit in the Receive and Transmit Configuration RAM.
10. Turns on HDLC channels.	Writing to all necessary TFDA1 bits of the TP[n]CR registers to 1 to allow ports to transmit normally.
11. Have enough time for all configurations to take effect.	It is going to take a minimum of 500 µs or 768 RC & TC clock cycles (which ever is longer) before packet data can be processed.

NOTE

It is recommended that a "Hardware Reset" be applied to the DS3134 upon power on.

Table 1. Indirect Registers

Register Name (Acronym)	Number of Indirect Registers
Channelized Port registers (CP0RD to CP15RD)	6144 (16 Ports x 128 DS0 Channels x 3 Registers for each DS0 Channel)
Receive HDLC Channel Definition register (RHCD)	256 (one for each HDLC Channel)
Transmit HDLC Channel Definition register (THCD)	256 (one for each HDLC Channel)
Receive DMA Configuration register (RDMAC)	1536 (one for each HDLC Channel)
Transmit DMA Configuration register (TDMAC)	3072 (one for each HDLC Channel)
Receive FIFO Staring Block Pointer register (RFSBP)	256 (one for each HDLC Channel)
Receive FIFO Block Pointer register (RFBP)	1024 (one for each FIFO Block)
Receive FIFO High Water Mark register (RFHWM)	256 (one for each HDLC Channel)
Transmit FIFO Staring Block Pointer register (TFSBP)	256 (one for each HDLC Channel)

Transmit FIFO Block Pointer register (TFBP)	1024 (one for each FIFO Block)
Transmit FIFO Low Water Mark register (TFLWM)	256 (one for each HDLC Channel)

More Information

DS3134: QuickView -- Full (PDF) Data Sheet -- Free Samples